

FIG. 1

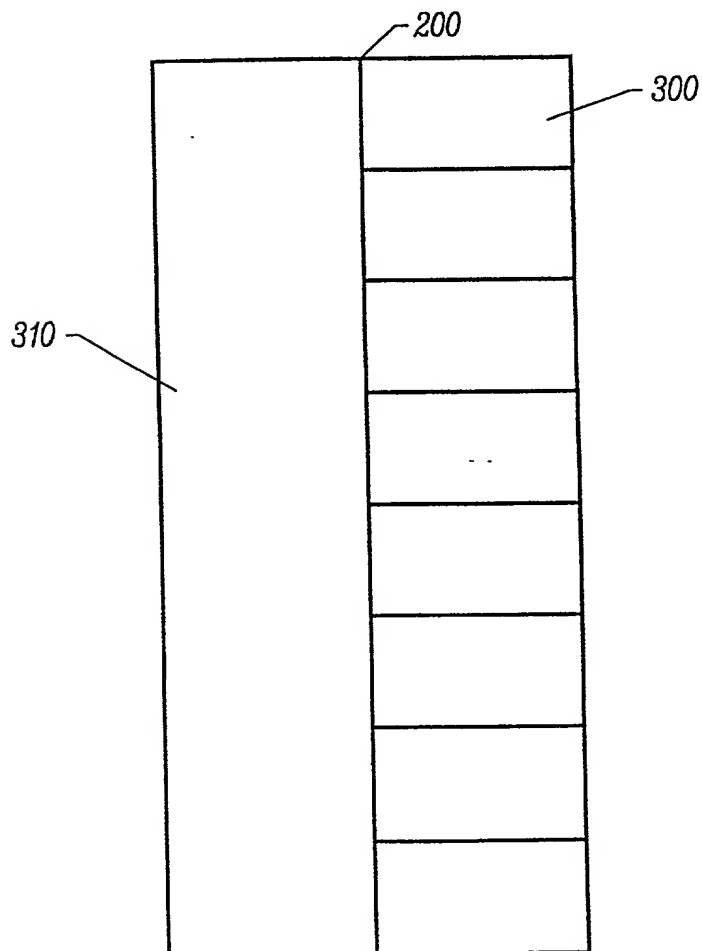


FIG. 3

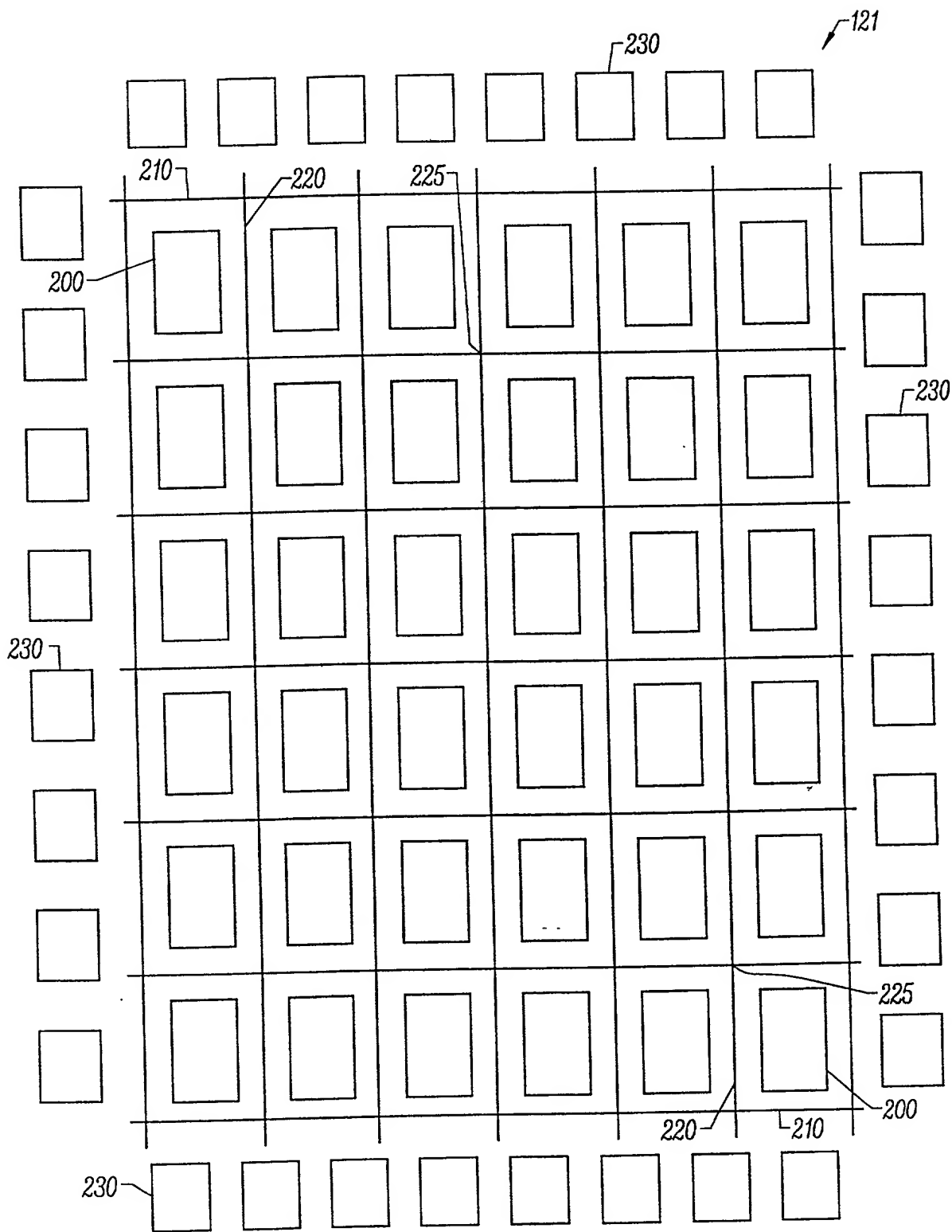


FIG. 2

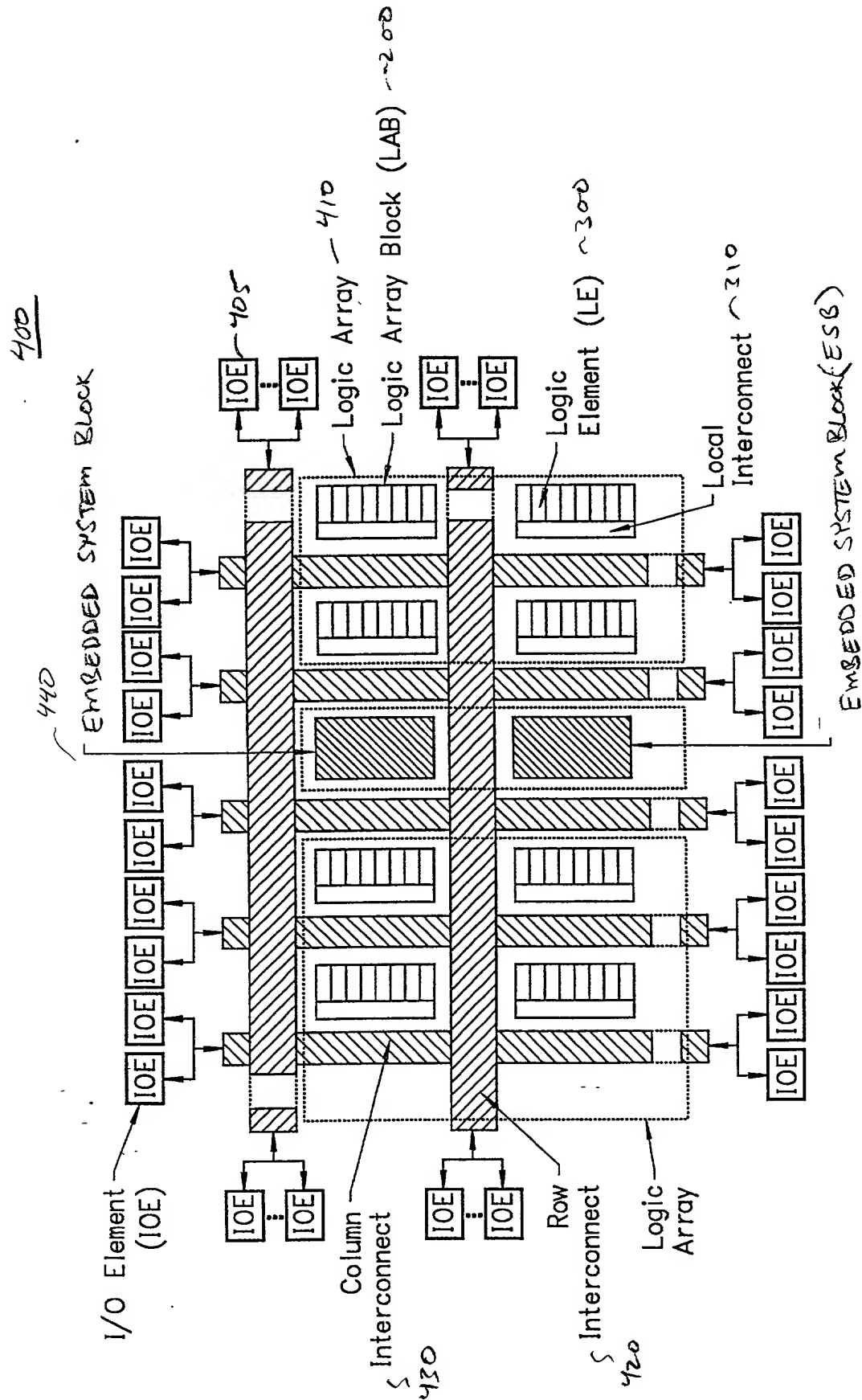


FIG. 4

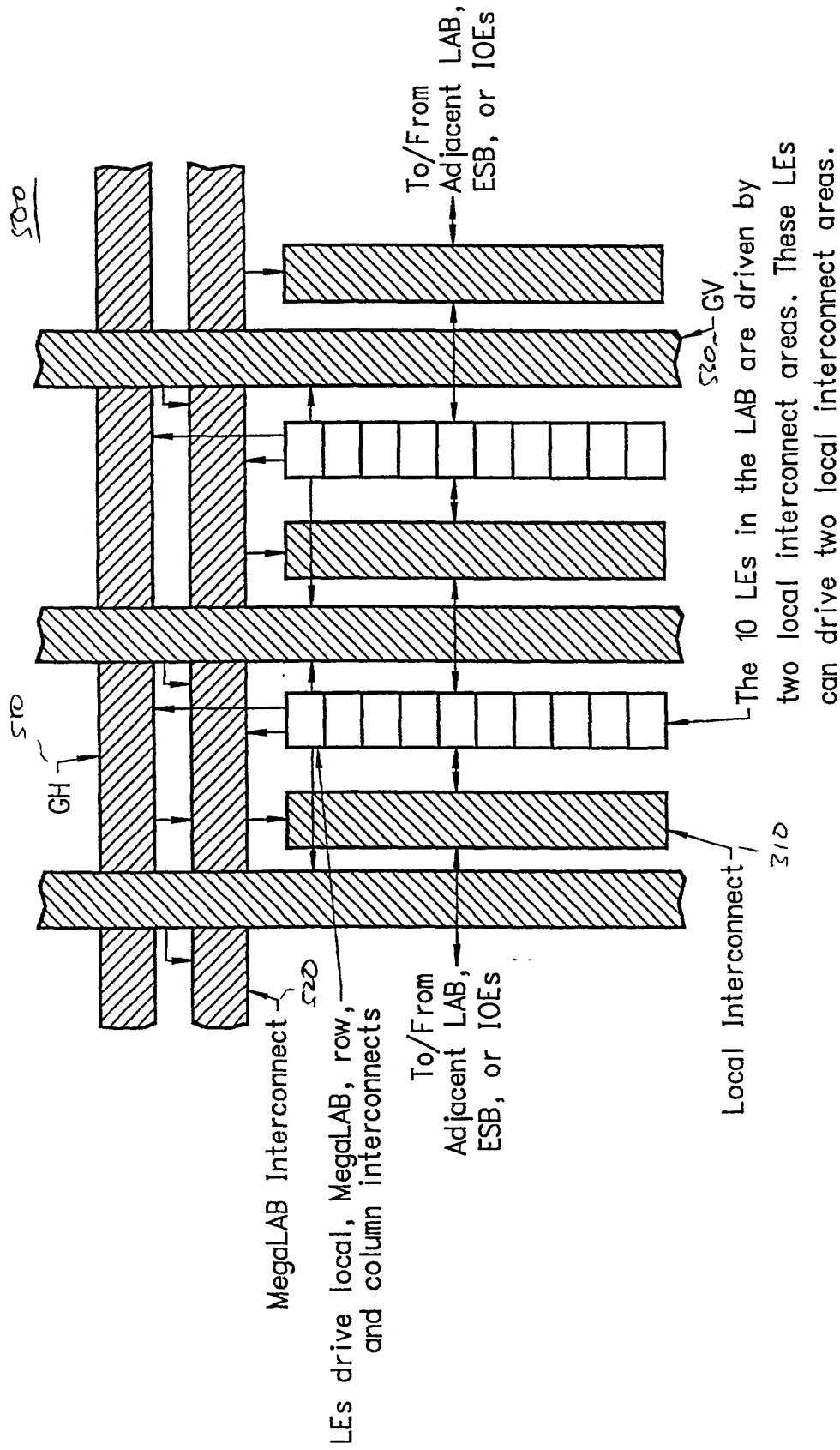


FIG. 5

600

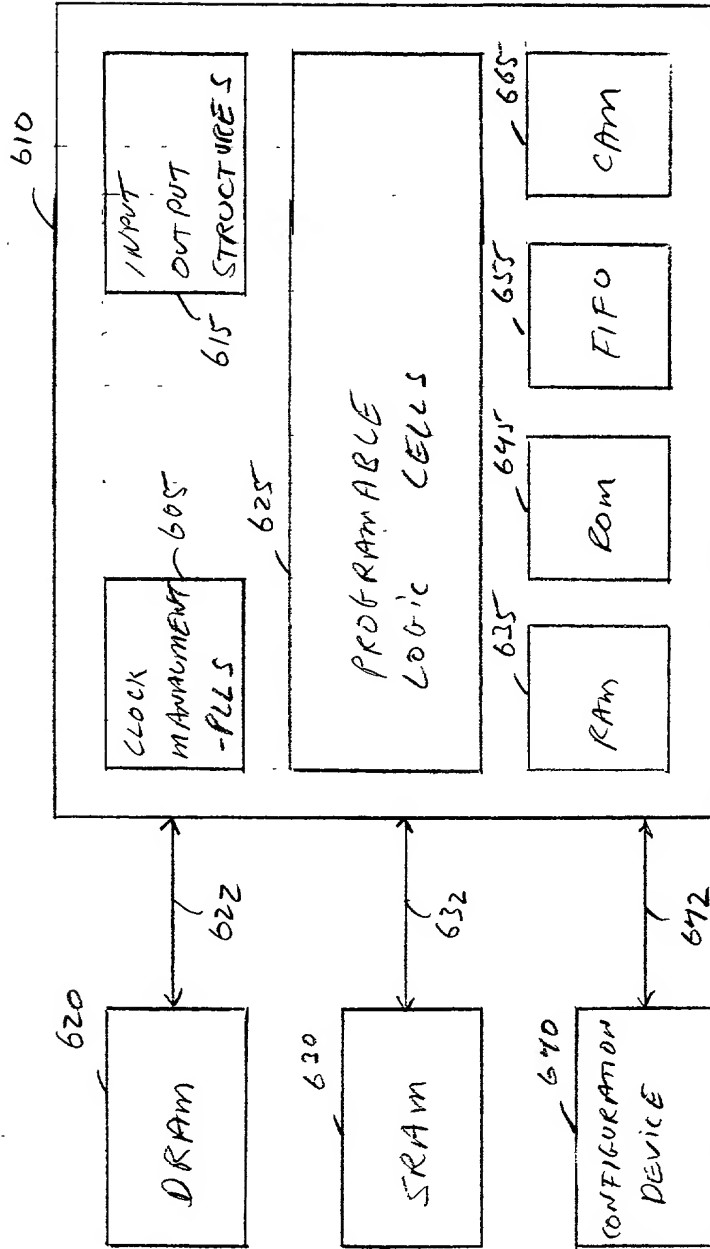


FIGURE 6

700

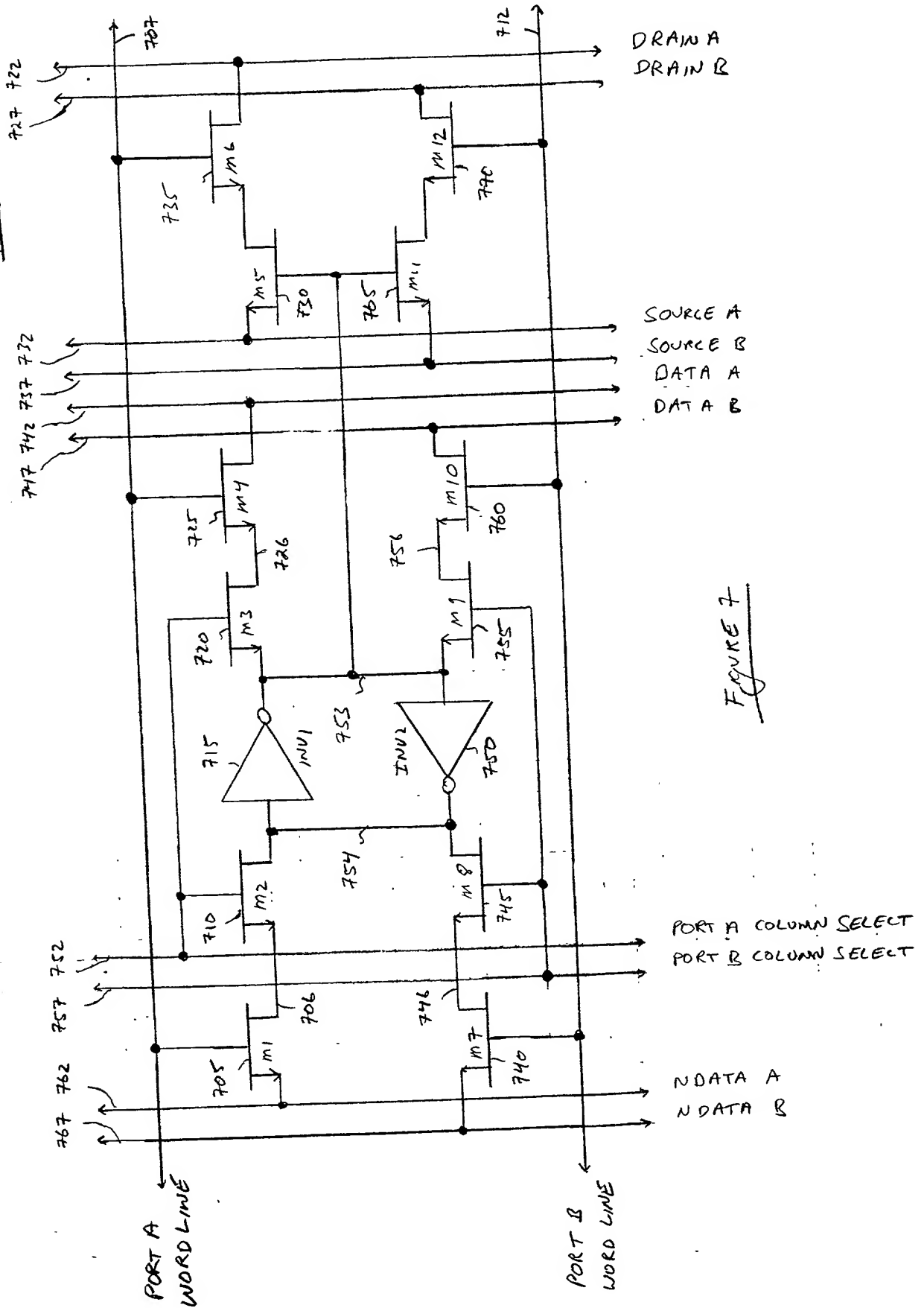


FIGURE 7

204470 56534001

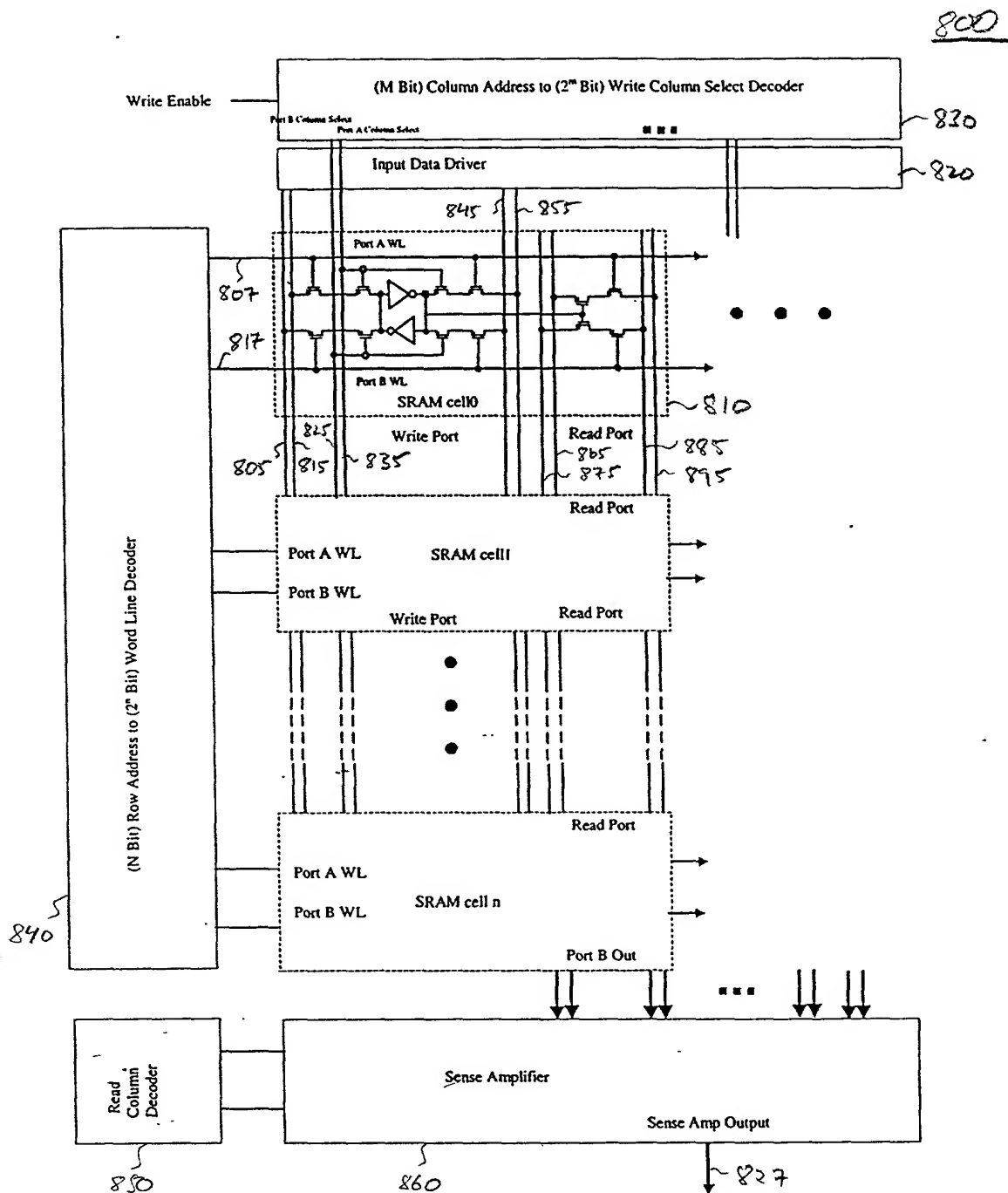


FIGURE 8

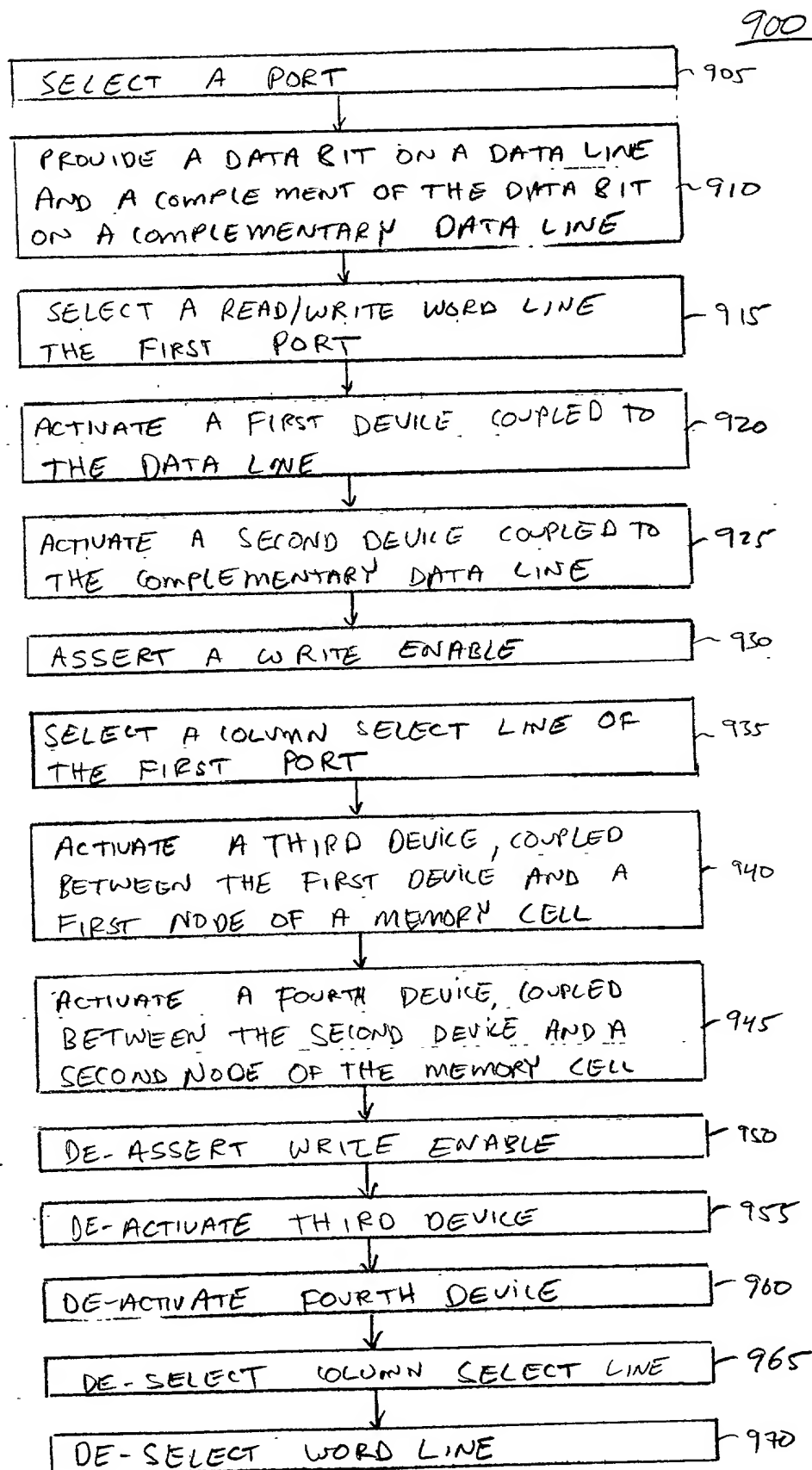


FIGURE 9



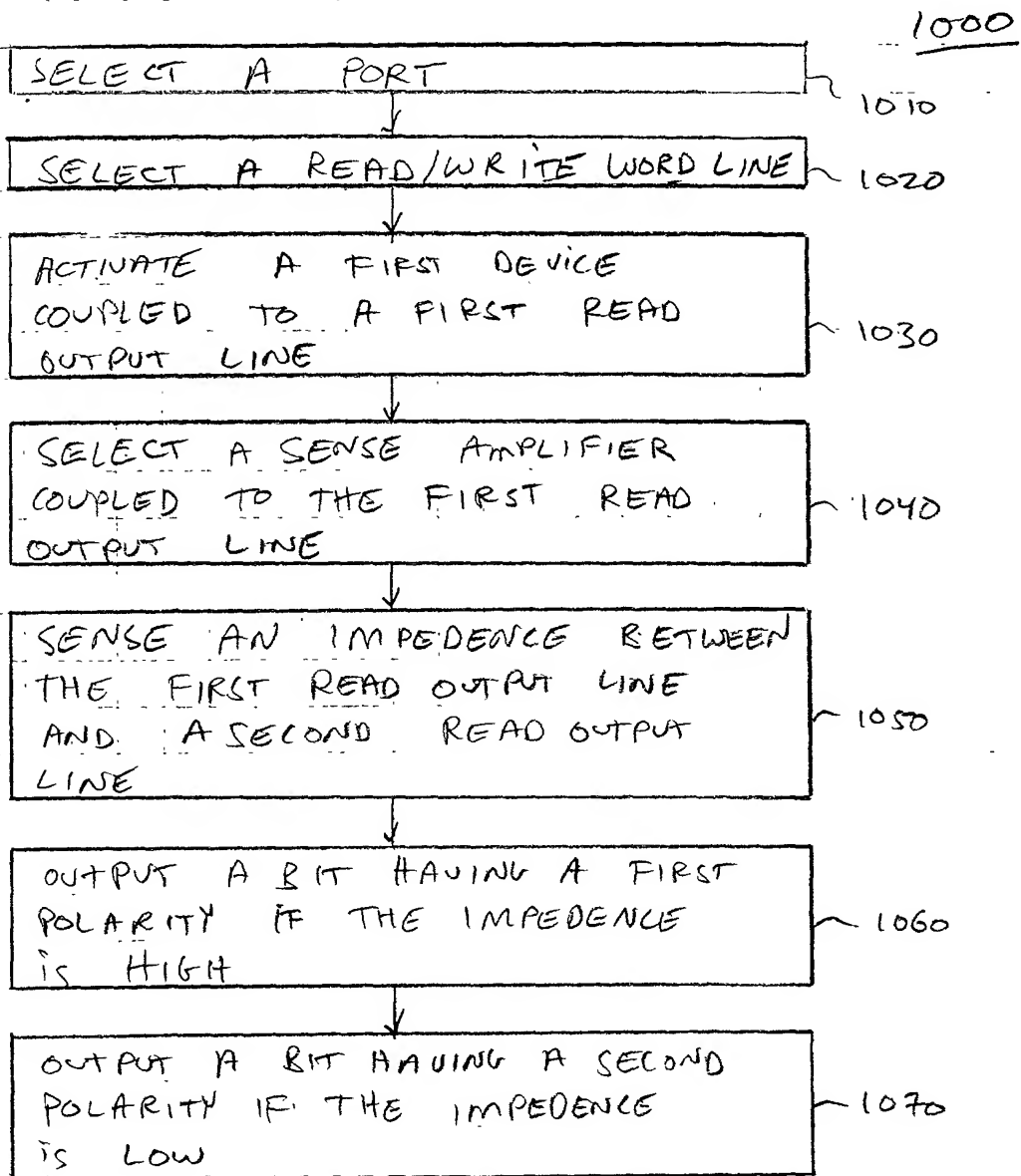


FIGURE 10

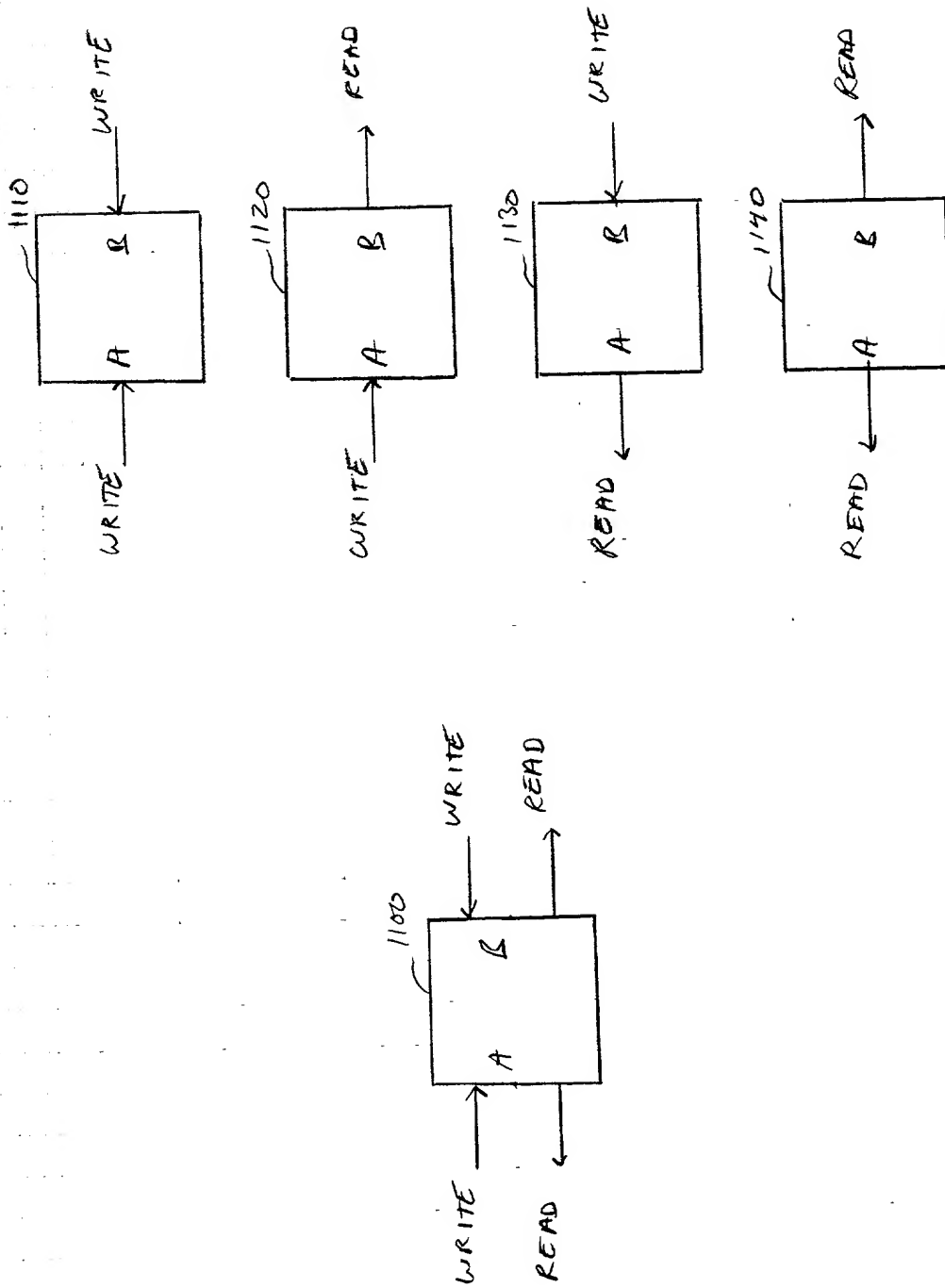


Figure 11

WRITE A NUMBER OF DATA ENTRIES,  
EACH DATA ENTRY IN ONE COLUMN,  
WHERE THE DATA ENTRY IS WRITTEN  
TO THE ODD NUMBERED MEMORY CELLS,  
AND A COMPLEMENT OF THE DATA  
ENTRY IS WRITTEN TO THE EVEN  
NUMBERED CELLS IN THE COLUMN

1200

1210

PROVIDE A COMPARAND AT THE  
MEMORY WORD LINES, THE  
COMPARAND DRIVING THE EVEN  
WORD LINES, AND A COMPLEMENT  
OF THE COMPARAND DRIVING THE  
ODD WORD LINES

1220

DETERMINE THE PARALLEL  
IMPEDENCE OF THE READ CELLS  
IN THE COLUMN

1230

FOR EACH COLUMN IN MEMORY,  
OUTPUTTING A BIT HAVING A  
FIRST POLARITY IF THE IMPEDENCE  
IS HIGH

1240

FOR EACH COLUMN IN MEMORY,  
OUTPUTTING A BIT HAVING A  
SECOND POLARITY IF THE IMPEDENCE  
IS LOW

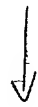
1250

FIGURE 12

$$\text{PRODUCT TERM} = A \cdot B \cdot \overline{C}$$

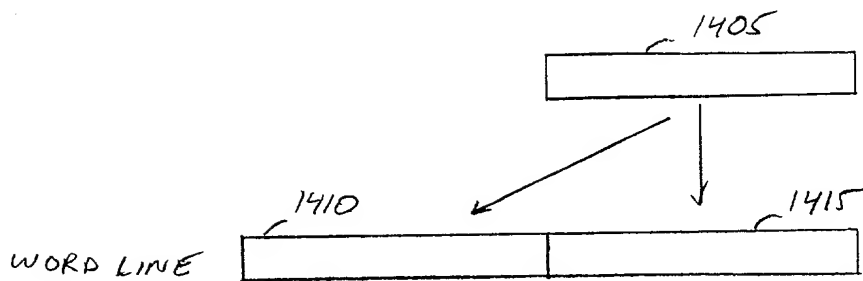
A "MATCH" OCCURS WHEN  $A=1, B=1, C=0$

COMPARAND INPUT		PRODUCT TERM STORED IN MEMORY	
1340	0	1	A
	1 →	0	$\overline{A}$
	0	1	B
	1 →	0	$\overline{B}$
	1 →	0	C
	0	1	$\overline{C}$



HIGH IMPEDENCE AT  $\sim 1350$   
SENSE AMPLIFIER  
INPUT

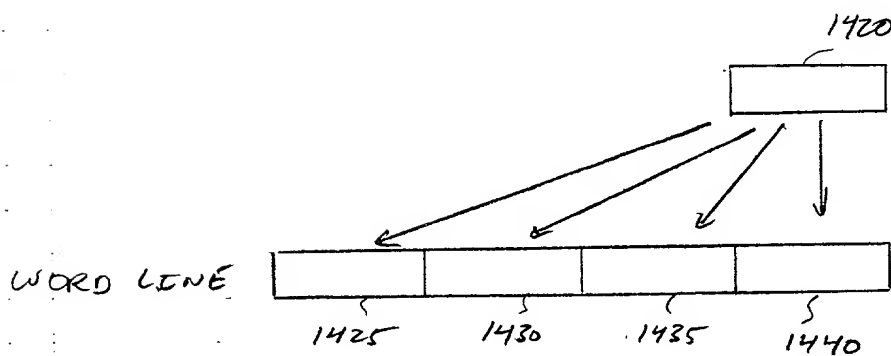
FIGURE 13



DATA TO  
BE WRITTEN

1:2  
ONE EXTRA  
ADDRESS BIT

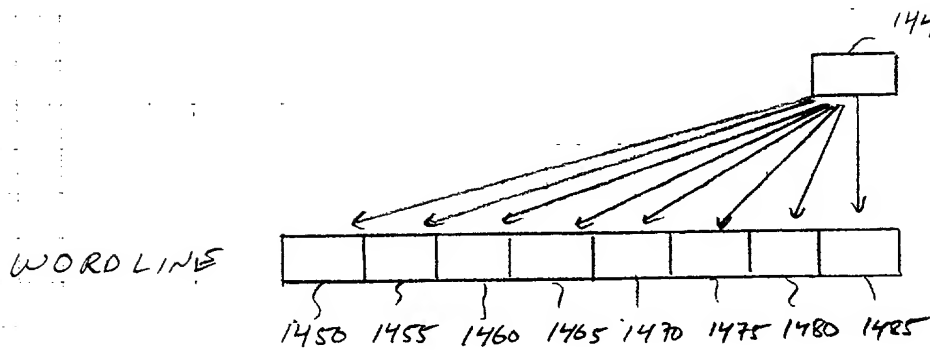
FIGURE 14A



DATA TO  
BE WRITTEN

1:4  
TWO EXTRA  
ADDRESS BITS

FIGURE 14B



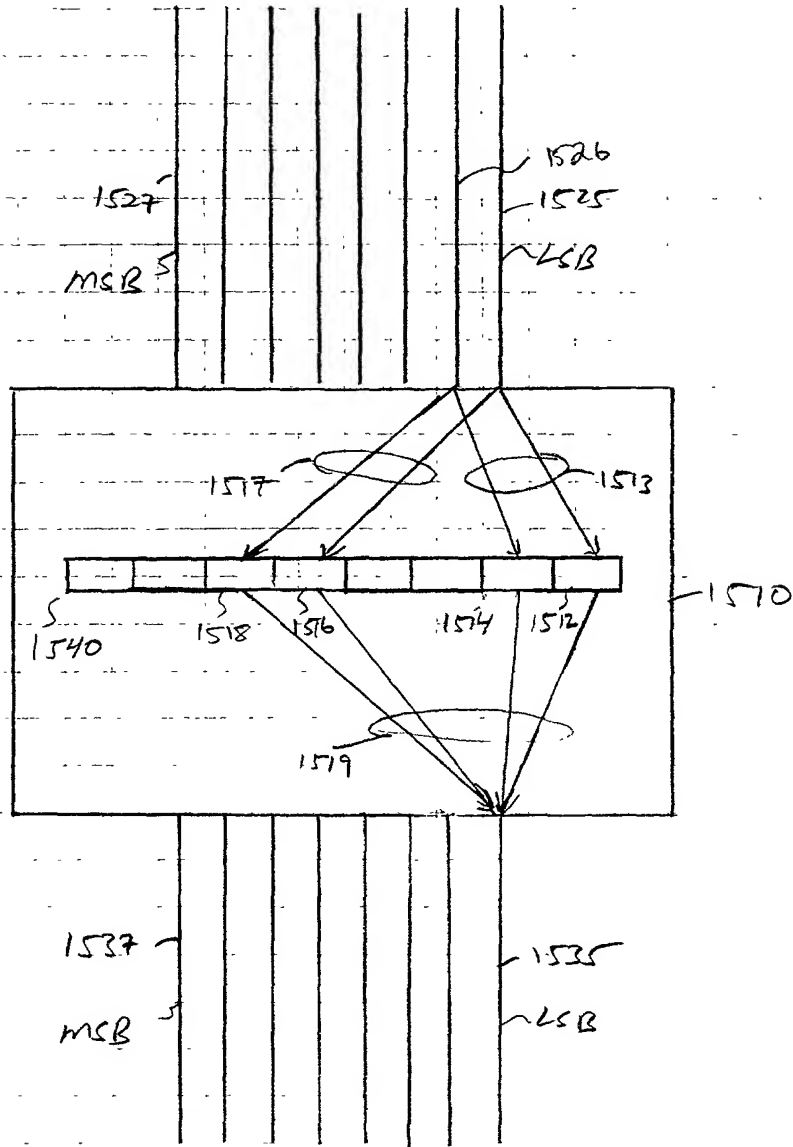
DATA TO  
BE WRITTEN

1:8  
THREE EXTRA  
ADDRESS BITS

FIGURE 14C

INPUT DATA BUS ~ 1520

1500



OUTPUT DATA BUS ~ 1530

FIGURE 15

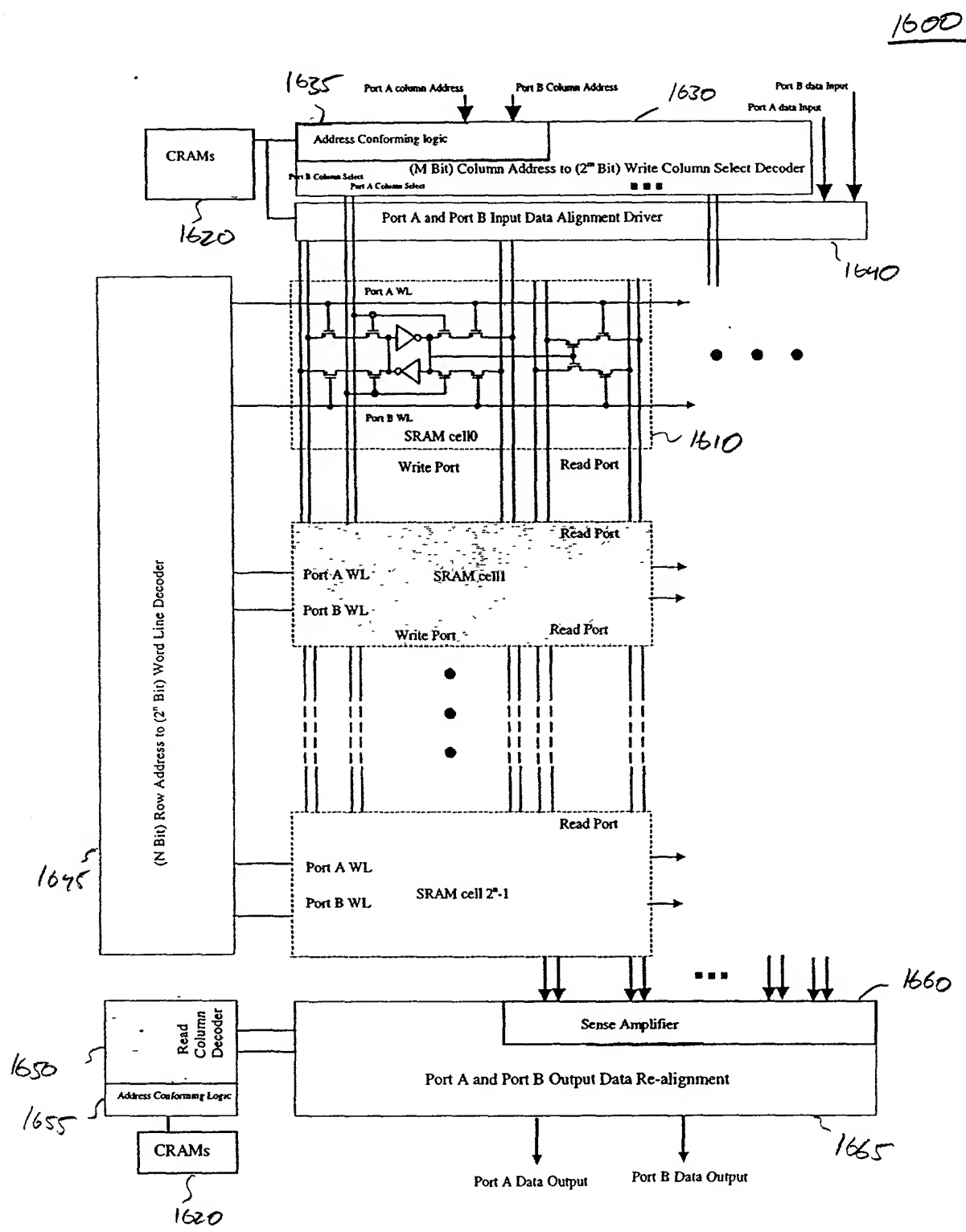
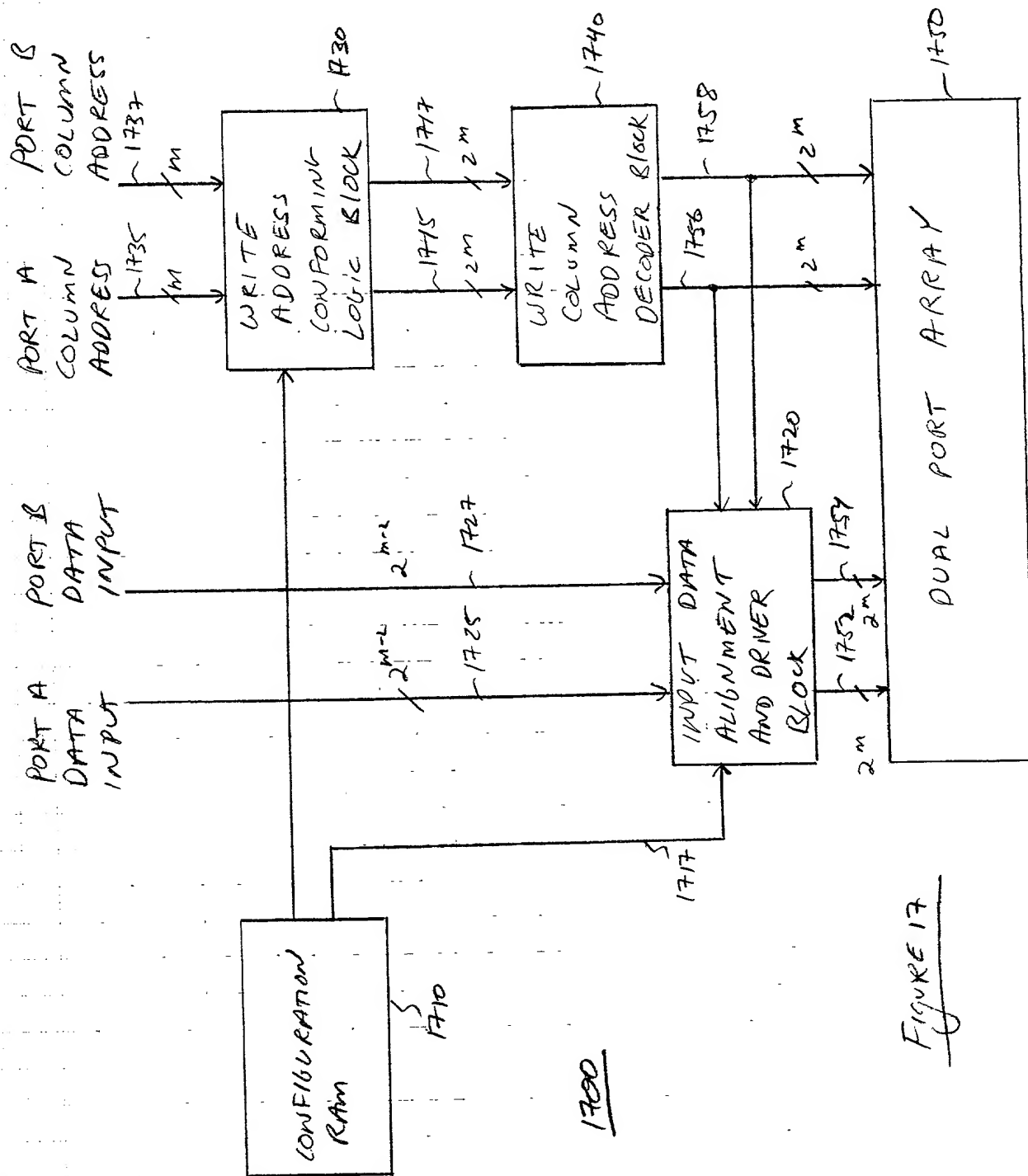


Figure 16



1700

FIGURE 17



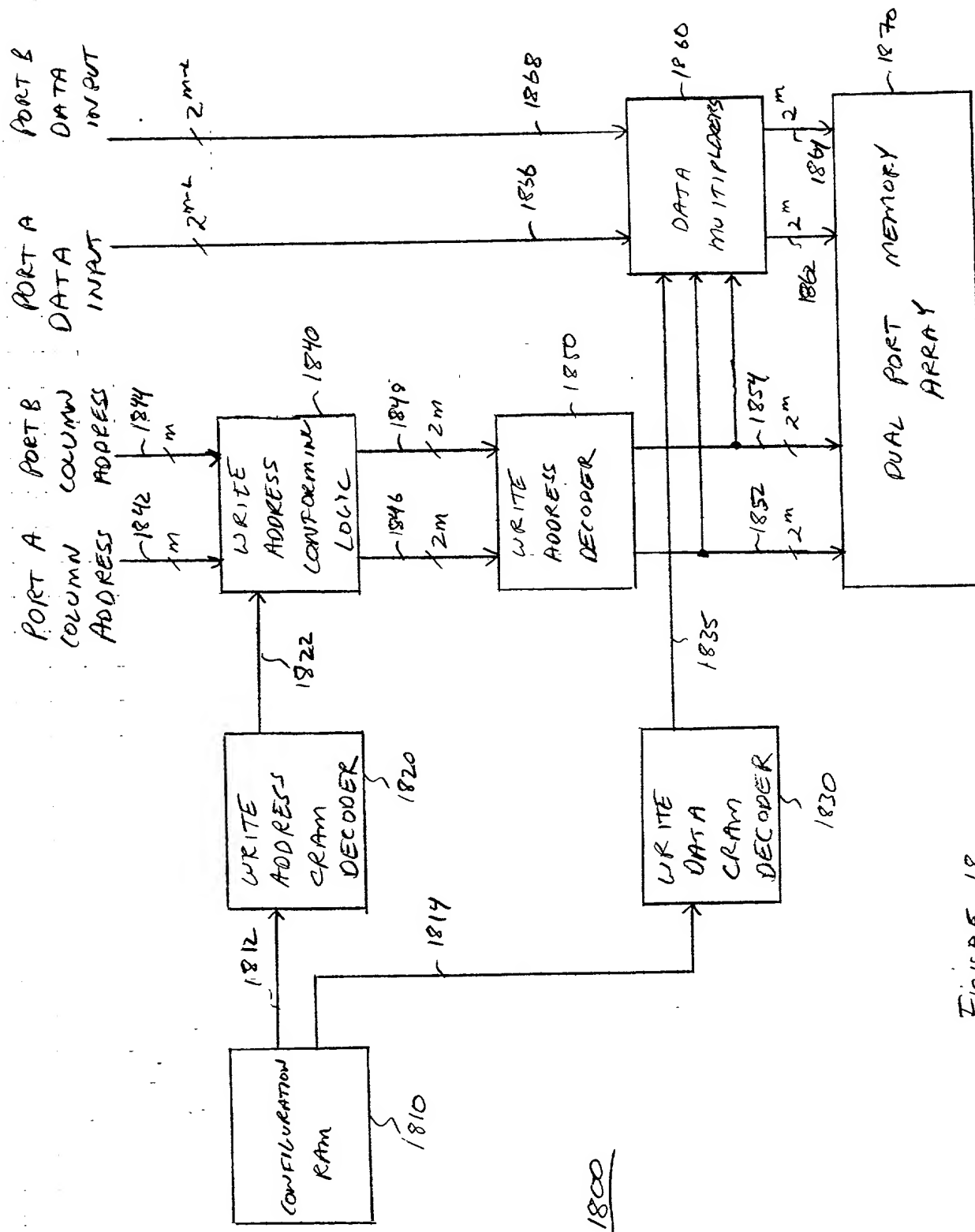


Figure 18

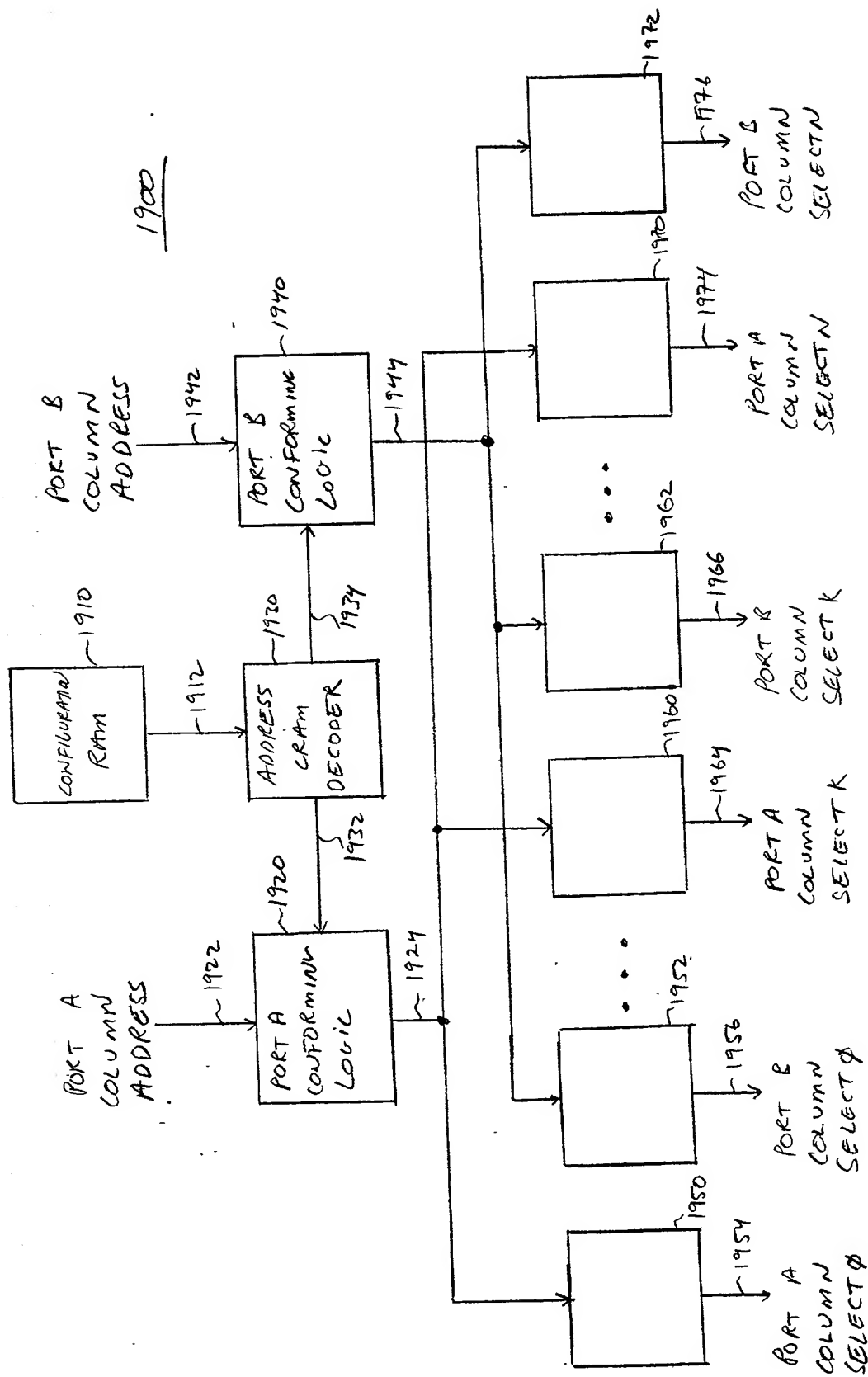


Figure 19

2000

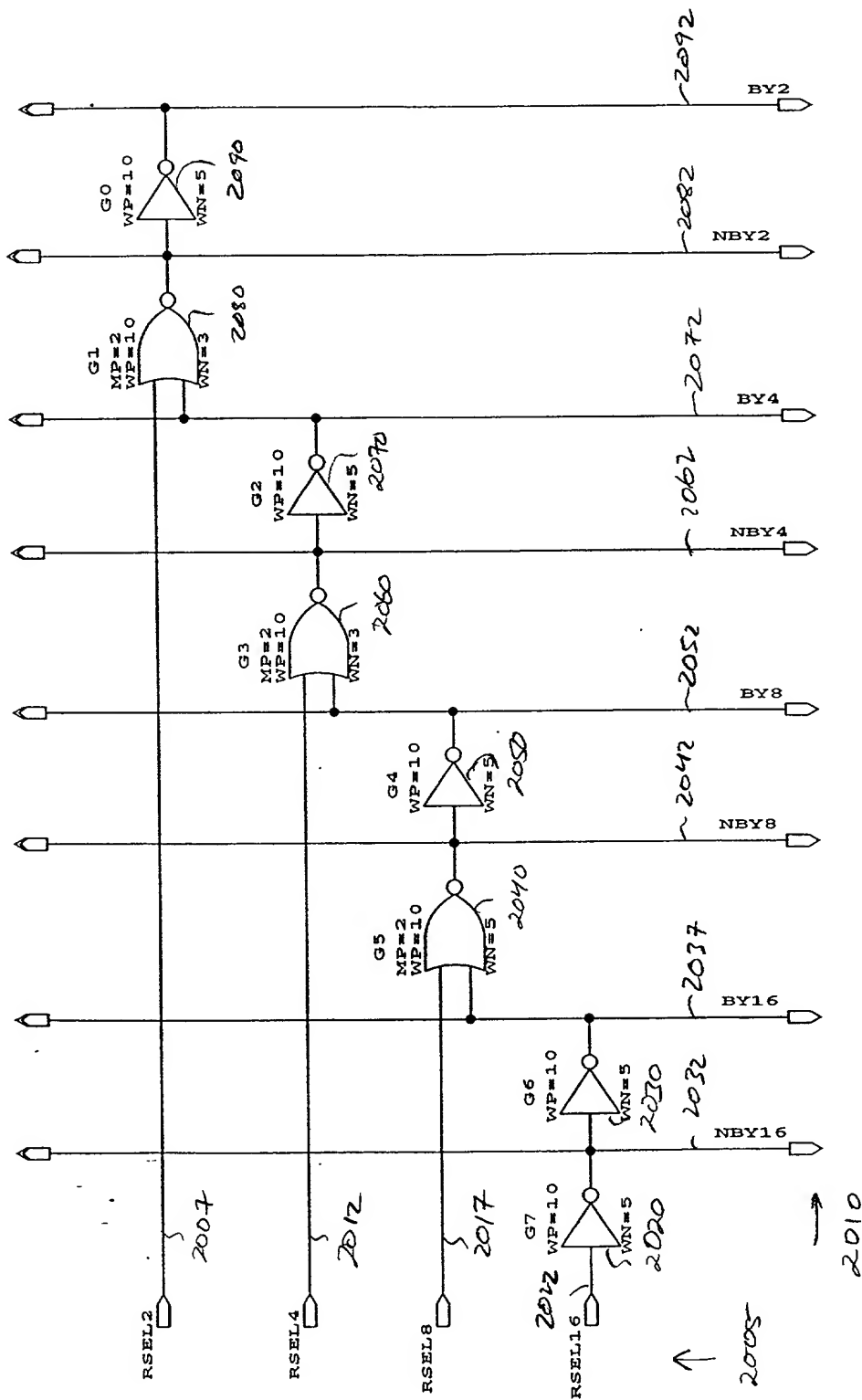


Figure 20

204470" 6664001

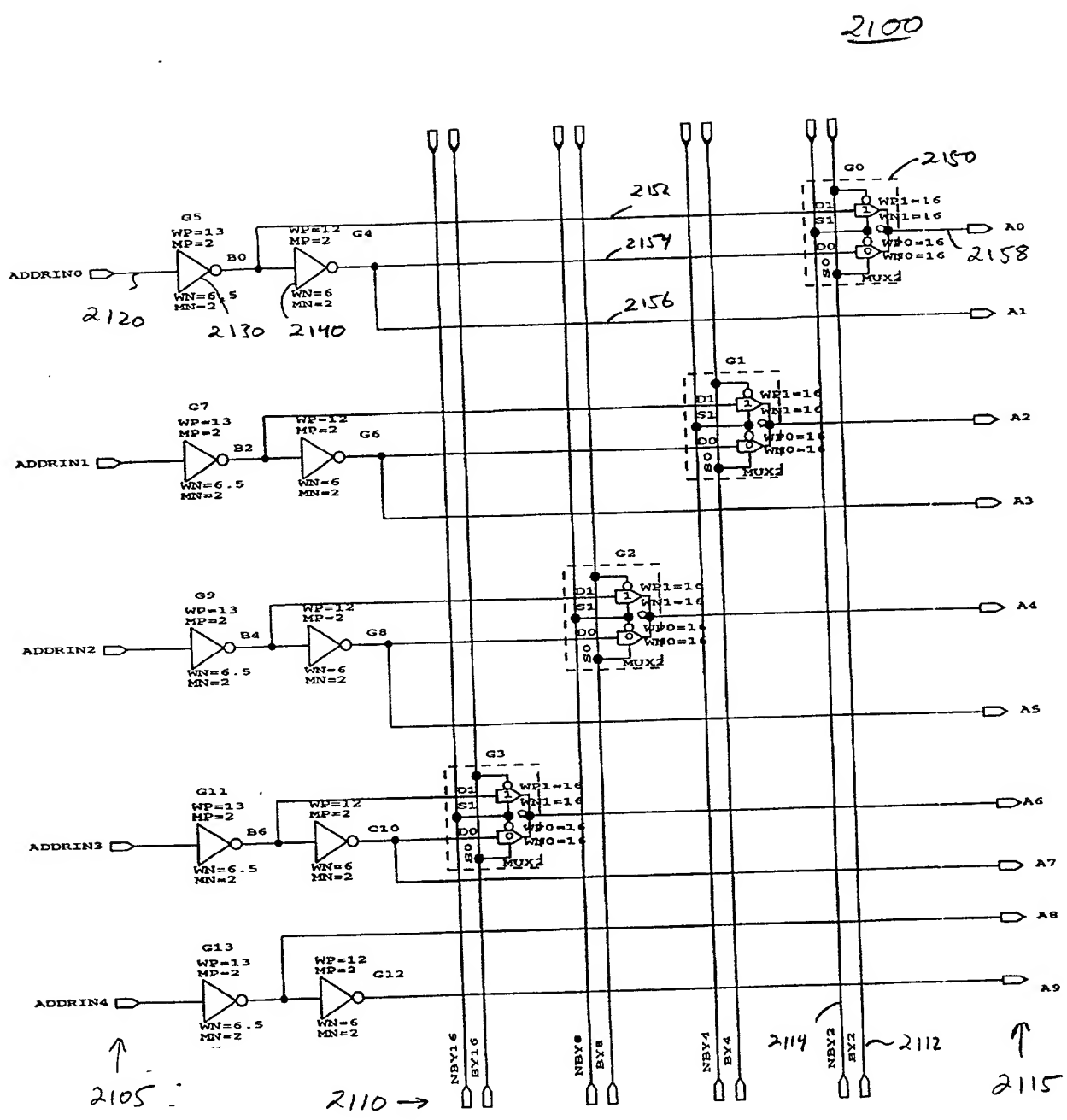
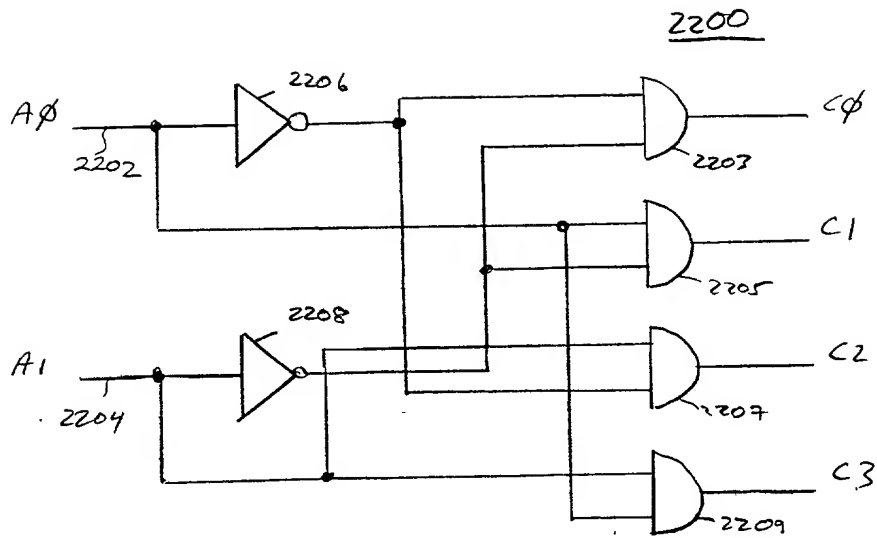


Figure 21



2210

$A1$	$A\phi$	$C\phi$	$C1$	$C2$	$C3$
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

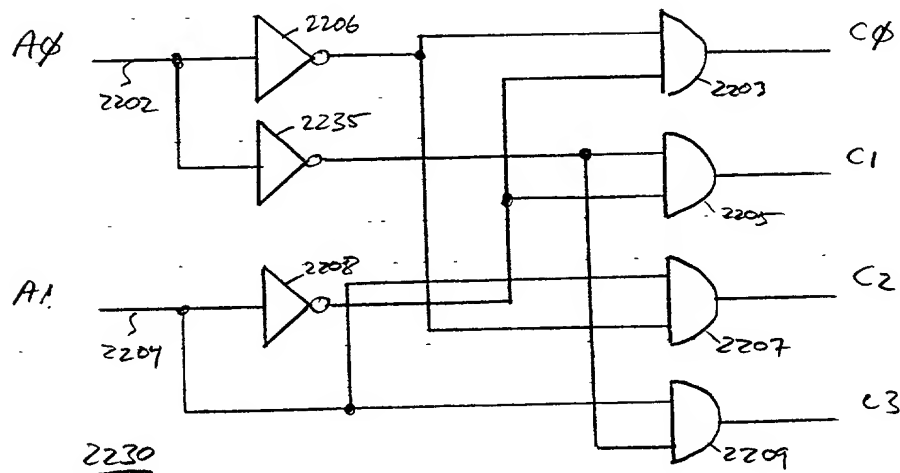
2220

$$C\phi = \overline{A1} \cdot \overline{A\phi}$$

$$C1 = \overline{A1} \cdot A\phi$$

$$C2 = A1 \cdot \overline{A\phi}$$

$$C3 = A1 \cdot A\phi$$



2240

$$C\phi = \overline{A1} \cdot \overline{A\phi}$$

$$C1 = \overline{A1} \cdot A\phi$$

$$C2 = A1 \cdot \overline{A\phi}$$

$$C3 = A1 \cdot A\phi$$

2250

$A1$	$A\phi$	$C\phi$	$C1$	$C2$	$C3$	
0	0	1	1	0	0	~2252
0	1	0	0	0	0	~2254
1	0	0	0	1	1	~2256
1	1	0	0	0	0	~2258

FIGURE 22

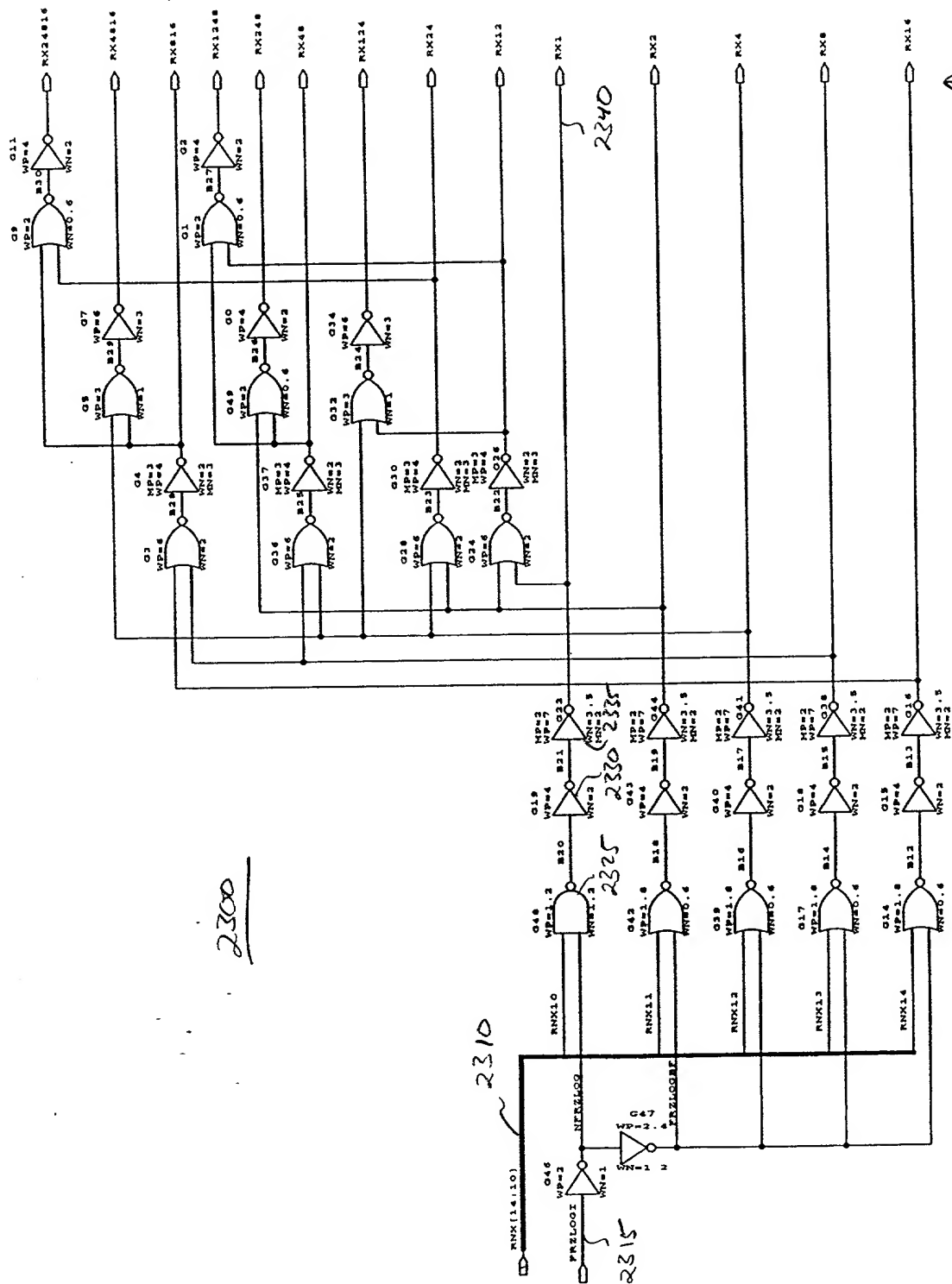
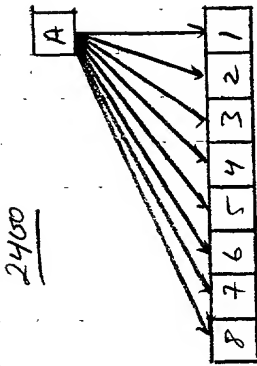
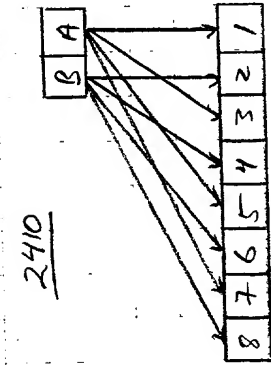
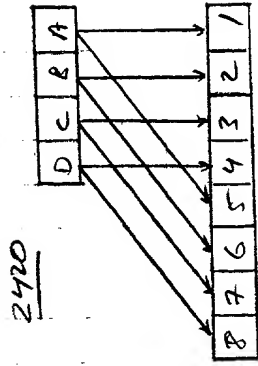


Figure 23



2432      2434      2436      2438

# BITS/WORD

2430

MUX	1	2	4	INPUTS	TYPE MUX
1	A	A	A	A	1:1
2	A	B	B	A, B	2:1
3	A	A	C	A, C	2:1
4	A	B	D	A, B, D	3:1
5	A	A	A	A	1:1
6	A	B	B	A, B	2:1
7	A	A	C	A, C	2:1
8	A	B	D	A, B, D	3:1

2446

2440

MUX	1	2	4	OUTPUTS	TYPE MUX
A	8, 7, 6, 5, 4, 3, 2, 1				1:8
B	8, 6, 4, 2				1:4
C	7, 3				1:2
D	8				1:1

Figure 24

204439-01400

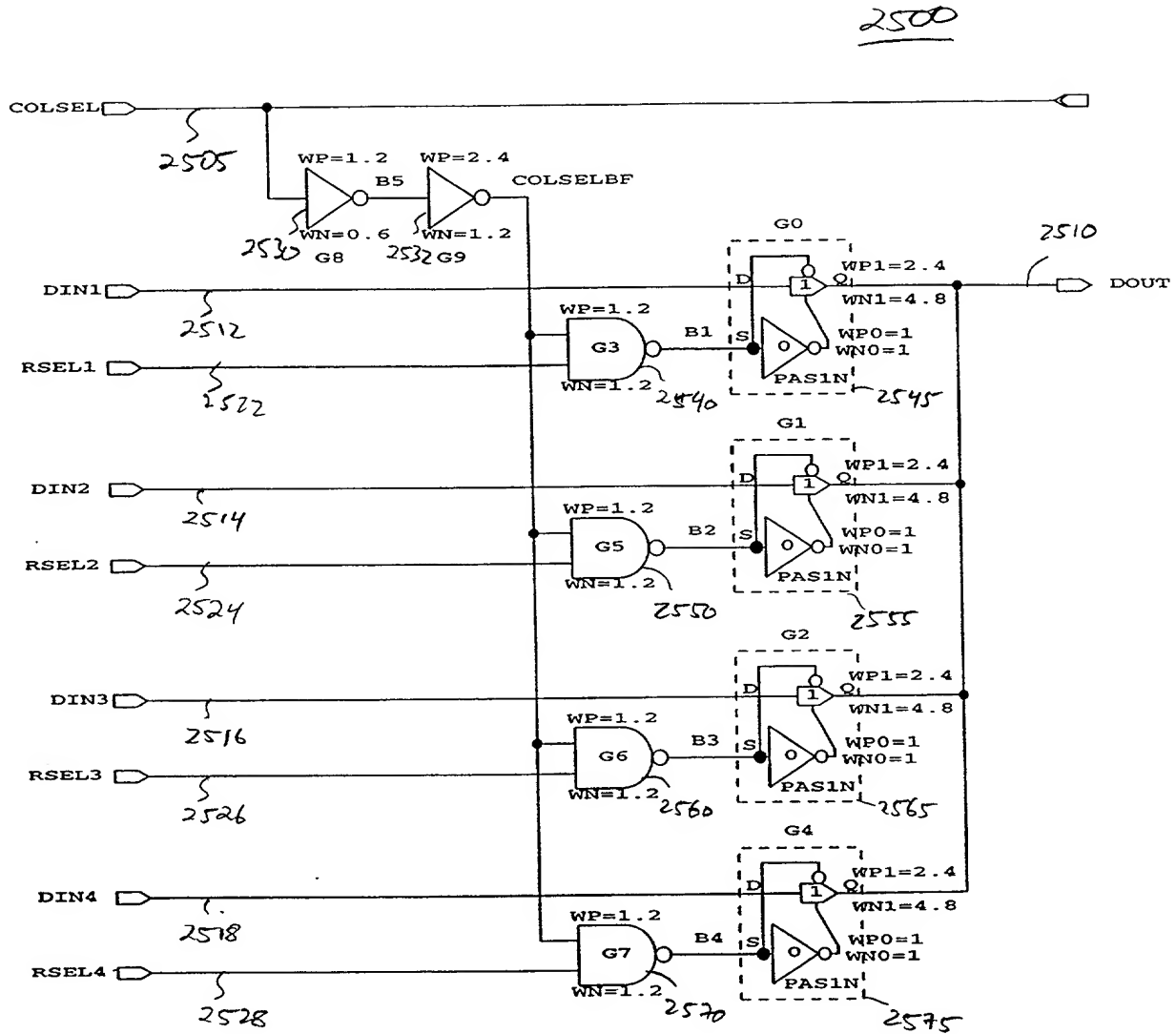


FIGURE 25



2600

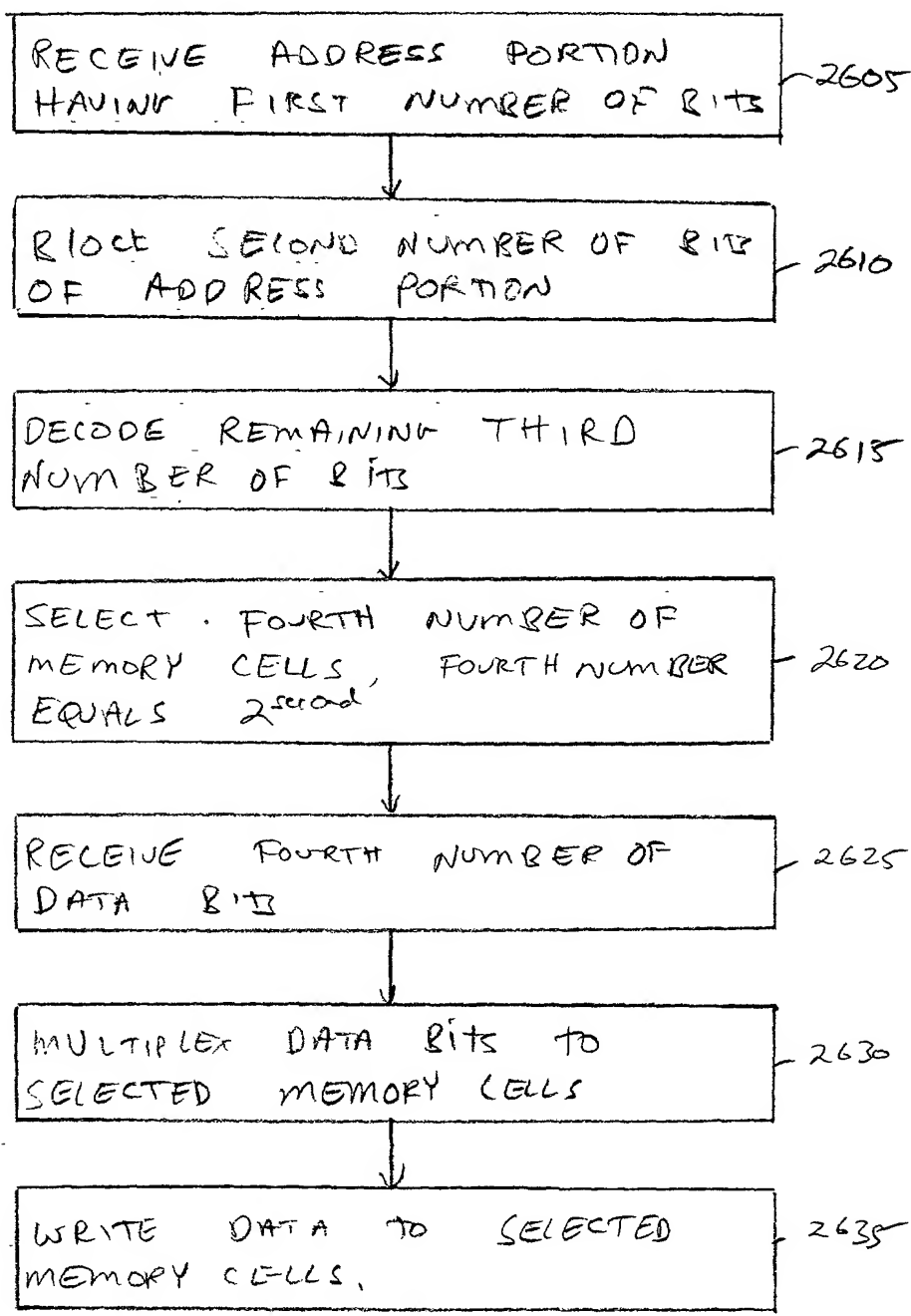


FIGURE 26

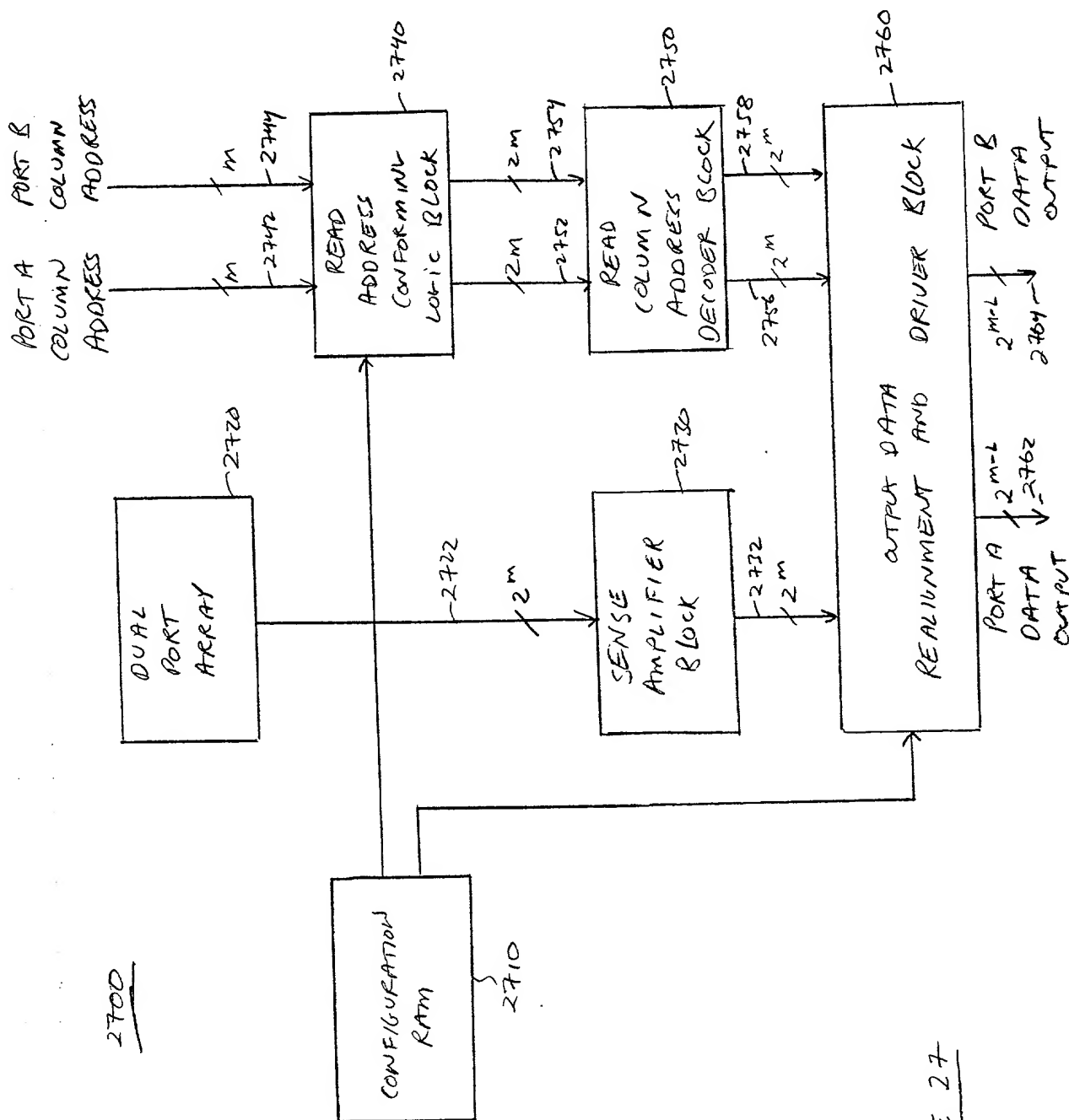


Figure 27

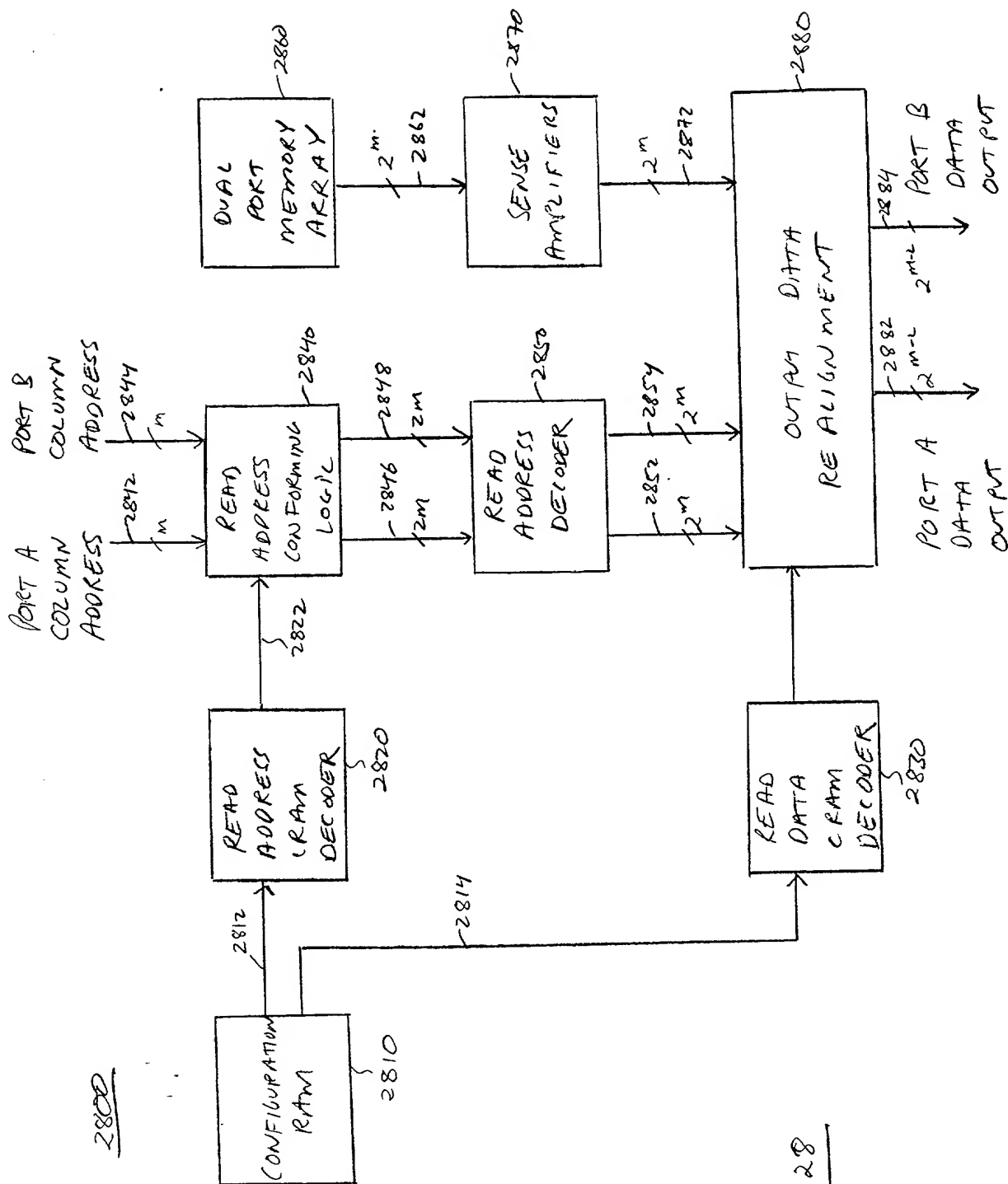
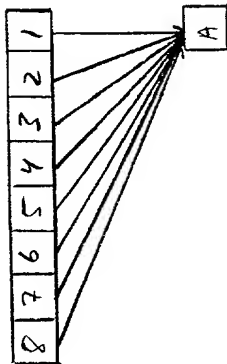
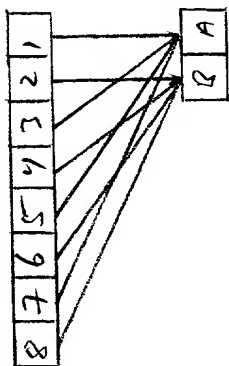


FIGURE 28

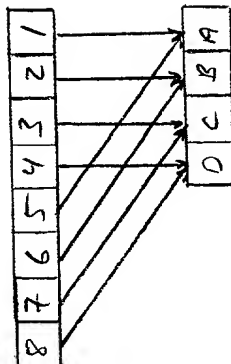
2900



2910



2920



2930

2932  
#bits / word

2934  
- 2936

2938  
- 2936

MUX	1	2	4	OUTPUTS	TYPE MUX
1	A	A	A	A	1:1
2	A	B	B	A, B	1:2
3	A	A	C	A, C	1:2
4	A	B	D	A, B, D	1:3
5	A	A	A	A	1:1
6	A	B	B	A, B	1:2
7	A	A	C	A, C	1:2
8	A	B	D	A, B, D	1:3

2940

2942  
- 2944

2946  
- 2946

MUX	INPUTS	TYPE MUX
A	8, 7, 6, 5, 4, 3, 2, 1	8:1
B	8, 6, 4, 2	4:1
C	7, 3	2:1
D	8	1:1

Figure 29

1046939-0140

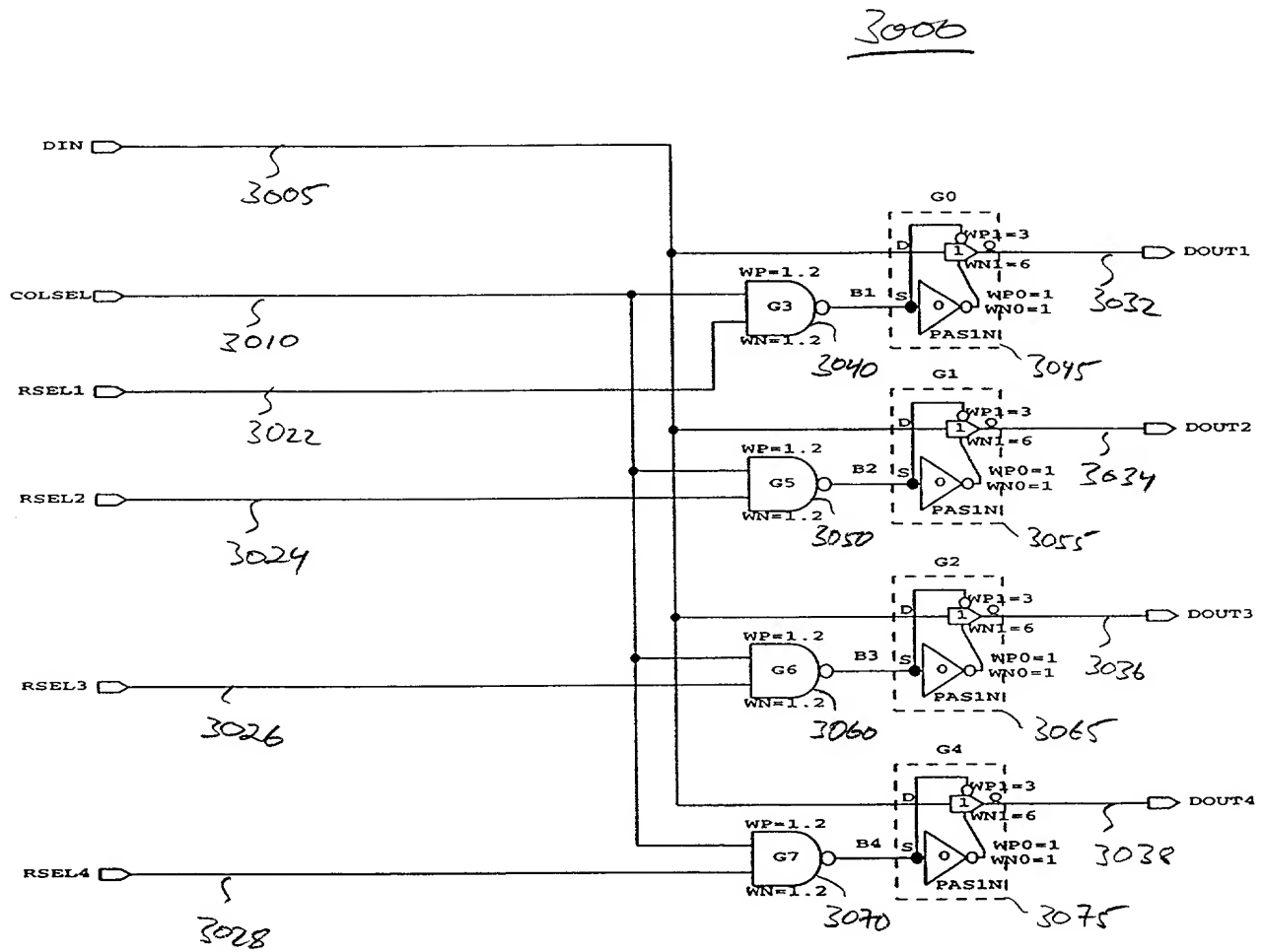


Figure 30

3100

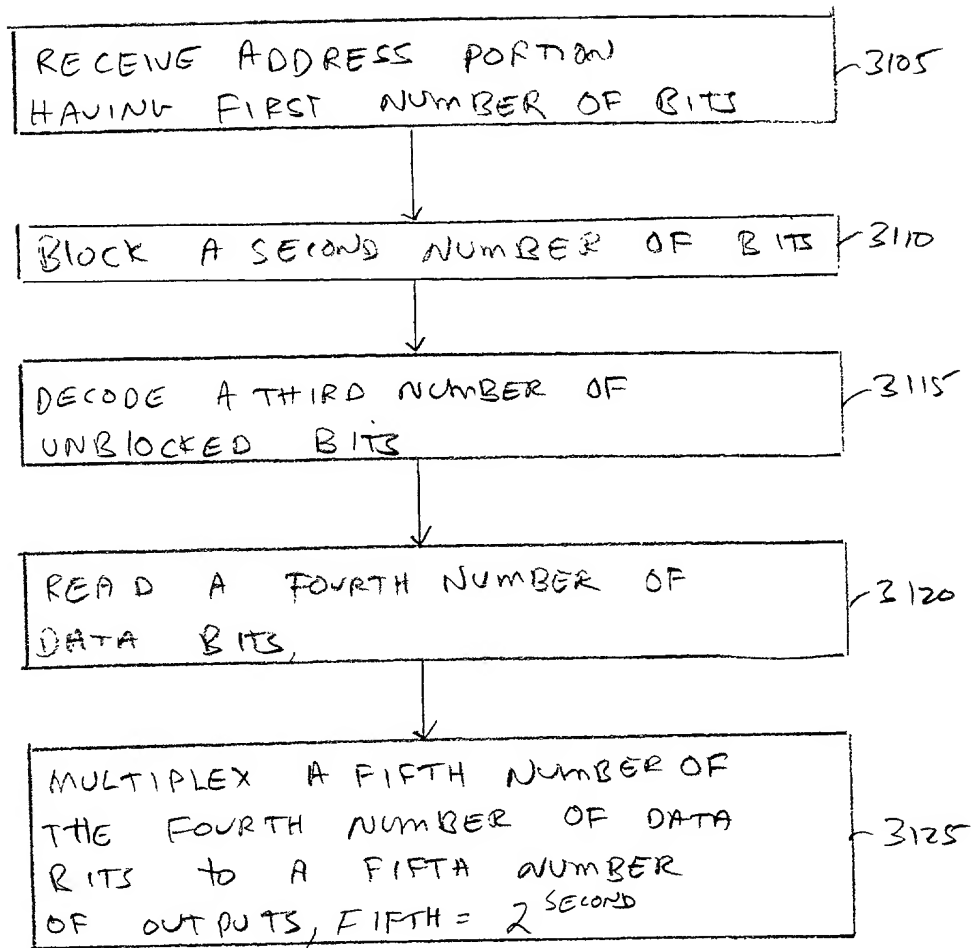


Figure 31